What is claimed is:

1. A method for fabricating a flash memory cell comprising:

depositing a pad oxide layer and a pad nitride layer on a semiconductor substrate;

patterning the pad nitride layer;

implanting ions into the substrate to form an ion implant region;

forming spacers on sidewalls of the pad nitride layer pattern;

removing some part of the pad oxide layer and the top portion of the substrate through an etching process using the spacers as a mask to form a trench that divides the ion implant region into two parts;

forming a gap filling insulating layer over the resulting substrate; and

forming a trench isolation layer and junction regions simultaneously by removing the spacers, the pad nitride layer pattern, the pad oxide layer, and the top portion of the gap filling insulating layer.

2. The method as defined by claim 1, wherein the spacers are formed of a material selected from the group consisting of nitride and TEOS (tetraethyl orthosilicate) oxides.

3. The method as defined by claim 1, wherein the pad oxide layer functions as a screen oxide layer during the ion implantation.

4. The method as defined by claim 1, wherein the ion implanted is one of As and P.

5. The method as defined by claim 1, wherein the spacers have a thickness between about 500Å and 1500Å.

6. The method as defined by claim 1, further comprising performing a thermal treatment process for the densification of the gap filling insulating layer and the activation of the ion implant region.